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UNITED STATES PATENT APPLICATION FOR
PROCESS FOR REDUCING LEAKAGE IN AN INTEGRATED CIRCUIT
WITH SHALLOW TRENCH ISOLATED ACTIVE AREAS

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PROCESS FOR REDUCING LEAKAGE IN AN INTEGRATED CIRCUIT
WITH SHALLOW TRENCH ISOLATED ACTIVE AREAS

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BACKGROUND OF THE INVENTION
FIELD OF THE INVENTION

The present invention relates to the field of semiconductor processing.

10 More specifically, the present invention relates to the isolation of active areas on a semiconductor wafer.

RELATED ART

Isolating adjacent active areas is a very essential requirement as device
15 dimensions are scaled down on an integrated circuit (IC). As the scaling gets down below 0.25 μm technology, the Local Oxidation of Silicon (LOCOS) isolation scheme fails because the thickness of the grown isolating oxide is not adequate for the narrow space. In addition, the large encroachment associated with the LOCOS scheme makes it difficult to get the required active area width.
20 LOCOS also has high temperature and long oxidation periods. Shallow Trench Isolation (STI) is widely used to isolate active areas in VLSI technologies with critical dimensions less than 0.25 μm . This method provides robust isolation when the space between P+ and N+ active areas gets down below about 0.80 μm since the thickness of the isolation regions is not significantly limited and the
25 encroachment is very small.

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The STI process used currently involves creation of trenches of depth of about 3000 angstroms to 4000 angstroms in silicon in regions where isolation spaces are to be formed. The pattern of the spaces is etched in a silicon nitride layer deposited on top of a pad oxide. After the formation of the trench pattern,
5 silicon dioxide is deposited by a Chemical Vapor Deposition (CVD) process to fill the trenches. The oxide is polished using the silicon nitride as the stopping layer. The nitride is then stripped off to get the pattern of the active areas with isolating oxide spaces.

10 Shallow Trench Isolation however, has its own problems nominally because the oxide in the isolating regions is not grown but deposited and the stress levels in this oxide can become very high. The stress levels may be increased further by the shape of the active/isolation pattern. Active areas with sharp bends or corners are more prone to problems with stress. This stress,
15 combined with the damage caused by plasma etch such as spacer etch lead to the formation of nucleation sites for dislocations. Bombardment by heavy ions such as arsenic during ion implantation can lead to dislocations in the silicon crystal in these sites. These dislocations at the surface when intersecting the source/drain to substrate P-N junctions can give rise to severe reverse leakage
20 in these junctions that can either seriously affect the functionality of a Static Random Access Memory (SRAM) cell or can give rise to very high standby current in the cell.

Stress induced defects are seen near poly lines. When a poly line crosses an active area, there is likely to be a gouge into the active area next to the poly edge due to the poly/spacer etch. The gouge may also generate some nucleation sites for dislocations. The extent of gouge and or dislocation generation is decided by the quality of the oxide at the edge of the active area, which is mainly the liner oxide. Depending on where the poly line intersects the active area, the extent of damage caused by the spacer etch may be different. When the active area is straight, the liner oxide grown after trench etch is stress free and hence may be able to withstand the poly/spacer etch better. On the other hand, when the active area has a corner, the liner oxide grown in this region has high stress and hence may be more prone to gouge when a poly line crosses the corner. Thus in a SRAM cell, a poly line crossing the corner of an active area may give rise to dislocations. This will lead to leakage in the N+ to P-substrate junctions which will lead to failure of the cell.

SUMMARY OF THE INVENTION

Accordingly, what is needed is a method and process for the fabrication of an isolation region in a semiconductor which will reduce or eliminate leakage between active areas. What is needed yet is a method and process in which
5 the fabrication time for an isolation region in a semiconductor is reduced. What is also needed is a method and process which allows the further shrinkage of integrated circuits to smaller sizes compatible with the next technology generation. The present invention provides these advantages and others not specifically mentioned above but described in the sections to follow.

10 A method and process are disclosed for the fabrication of an isolation region in a semiconductor crystal. The method and process may be used in the fabrication of isolation regions used for the separation of adjacent active areas in an integrated circuit. A shallow trench is created on the surface of the
15 semiconductor in regions where isolation spaces are to be formed. A layer of silicon dioxide (LINOX) is then grown over the surfaces of the trench. The LINOX covers roughened regions formed along the surfaces of the trench during its formation.

20 In one embodiment of the present invention, the liner oxidation recipe calls for growing the LINOX in the presence of oxygen and chlorine at a temperature of about 1000 degrees Centigrade. In one embodiment of the present invention, immediately following the growth of the LINOX, the

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temperature is increased to about 1050 degrees Centigrade for a period of time
sufficient in order to anneal the LINOX. The remaining volume of the trench is
then filled with silicon dioxide by Chemical Vapor Deposition (CVD). The
surface of the semiconductor is then polished to reveal the pattern of active
5 areas with isolating oxide regions.

In one embodiment of the present invention, the step of annealing the
LINOX provides a number of distinct advantages. First of all, annealing greatly
reduces stresses in the LINOX and in the surrounding semiconductor material.
10 Annealing also increases the density of the LINOX. Thus annealing increases
the LINOX resistance to damage or gouge during any subsequent etching; for
instance during a poly/spacer etch. This leads to a reduction in dislocations in
the semiconductor crystal and an attendant reduction in electrical leakage
around the isolation region. In one embodiment of the present invention, the
15 electrical leakage in a SRAM cell with shallow trench isolated active areas
having sharp corners is reduced. A more robust LINOX and a reduction in
electrical leakage around an isolation region allows for the further shrinkage of
integrated circuit dimensions. In one embodiment of the present invention, a
reduction in the dimensions of a Static Random Access Memory (SRAM) cell is
20 made possible. Furthermore, denuding and gettering of the semiconductor are
both accomplished during the annealing step which results in a shortening of
total processing time. Finally, since gouging of the LINOX no longer occurs

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates an exemplary Shallow Trench Isolation scheme in accordance with one embodiment of the present invention.

5 Figure 2 is the cross-sectional view of a single trench in accordance with one embodiment of the present invention.

10 Figure 3 illustrates a cross-sectional view showing the grown Liner Oxide (LINOX) applied to the walls of the trench, in accordance with one embodiment of the present invention.

15 Figure 4 illustrates a cross-sectional view showing silicon dioxide trench filler deposited by Chemical Vapor Deposition (CVD) in accordance with one embodiment of the present invention.

 Figure 5 is a process diagram of the recipe for annealing the LINOX in accordance with one embodiment of the present invention.

20 Figure 6 is a cross-sectional view showing a poly line passing over a Shallow Trench Isolation (STI) region in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the present invention, a process for reducing leakage in a SRAM cell with shallow trench isolated active areas, numerous specific details are set forth in order to provide a thorough
5 understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail, as not to unnecessarily obscure aspects of the present invention. For instance, the
10 substrate used could be silicon or could also be other substrate materials, such as SiGe.

Figure 1 illustrates an exemplary Shallow Trench Isolation (STI) scheme in accordance with one embodiment of the present invention. An integrated
15 circuit may be realized by locating active semiconductor devices in the active regions 110, 120 and 130. Electrical isolation of active regions may be realized by the formation of shallow trenches in the surface of the semiconductor substrate between the active regions, which may then be filled with silicon dioxide to form isolation regions 140. The minimization or elimination of
20 electrical leakage currents between active regions along a leakage path 150 is a primary objective. In the present invention, the process used to form isolation regions 140 results in a reduction in electrical leakage currents between active regions when compared with prior art methods. These and other advantages of

the present invention not specifically enumerated above will become clear within discussions of the present invention below.

Figure 2 is the cross-sectional view of a shallow trench 210 separating two active regions 220 and 230 in a semiconductor substrate 200 in accordance with one embodiment of the present invention. In one embodiment of the present invention, the trench may be formed by plasma etching. A small trench width 250 may be preferred to accommodate smaller integrated circuit geometry. A larger trench depth 260 may reduce electrical current leakage between active regions 220 and 230. The plasma etch used to form the trench results in uneven trench surfaces 240. These uneven surfaces lead to the formation of stress regions and dislocations in the active regions during subsequent processing steps as described below. Regions of stress and dislocations may in turn result in increased electrical leakage between active areas as well as active device failure. In one embodiment, the shallow trench having a width of at most $0.3\ \mu$ with fallback widths of $0.25\ \mu$ and $0.21\ \mu$.

In the present invention, a layer of silicon dioxide, referred to as the Liner Oxide layer (LINOX), may be grown over the inner surfaces of the trench to cover the unevenness and to reduce occurrences of dislocations. Figure 3 illustrates a cross-sectional view 300 showing the grown Liner Oxide (LINOX) 330 covering the uneven inner surfaces of the trench 340. The trench separates the two active regions 310 and 320. Since the LINOX 330 is grown, it

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becomes an integral part of the semiconductor substrate, as opposed to silicon dioxide that is deposited on the surface of the substrate by Chemical Vapor Deposition (CVD). Following the LINOX growth step, the temperature is elevated slightly for a period of time to anneal the LINOX 330. In one
5 embodiment of the present invention, the LINOX 330 may be grown at a temperature of 1000 degrees centigrade, and annealing of the LINOX 330 may be accomplished over a period of 3 hours at a temperature of 1050 degrees centigrade.

10 Annealing causes an increase in density of the LINOX 330 which increases its strength and relieves stresses which may form along the trench surfaces at corners or at sharp edges. The increased strength of the LINOX 330 causes it to be insensitive to subsequent processing steps. Relieving the stresses in the LINOX 330 (especially at the corners) may result in a reduction
15 in or elimination of dislocations in the semiconductor substrate which in turn may reduce electrical leakage currents between active areas. An additional advantage of the present invention is the accomplishment of denuding and gettering that occur during the annealing process.

20 Figure 4 illustrates a cross-sectional view 400 of a Shallow Trench Isolation (STI) region 450 separating two active regions 410 and 420. The silicon dioxide trench filler 430 may be deposited by Chemical Vapor Deposition (CVD) in accordance with one embodiment of the present invention.

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The LINOX 440 separates the deposited CVD oxide 430 from the semiconductor substrate active regions 410 and 420. As a result, the large stresses that occur when oxide is deposited by CVD directly into a trench without the LINOX may be eliminated. Thus the dislocations formed in the semiconductor substrate due to these stresses may also be eliminated in accordance with the present invention.

Figure 5 is an exemplary process diagram 500 which may be used to grow a liner oxide (LINOX) in a shallow trench on a semiconductor substrate in accordance with one embodiment of the present invention. At step 510, the semiconductor temperature is stabilized in the presence of Argon at 1000 degrees centigrade. In step 520, the LINOX is grown to the desired depth by holding the semiconductor at a temperature of 1000 degrees centigrade in the presence of oxygen and chlorine for a period of time. The semiconductor temperature is then increased in step 530 to 1050 degrees centigrade for a period of three hours to accomplish the annealing of the LINOX. During step 530, the density of the LINOX is increased density, stresses between the LINOX and the semiconductor substrate are relieved, and denuding and gettering are both accomplished. In step 540, the temperature is then reduced to the starting point of 800 degrees centigrade for further processing. It is appreciated that other possible gases besides Argon can be used, and also other possible sources of oxygen can be used.

occur as a result of the poly/spacer etch. In the present invention, annealing of the LINOX in the trench 820 reduces or eliminates gouging during poly/spacer etch. As a result, dislocations are eliminated which reduces electrical current leakage between active regions. Furthermore, limitations on the layout of poly lines are relaxed since annealing the LINOX has eliminated the gouging problem.

Figure 9 is the cross-sectional view 900 of an active area 930 separated by two isolation regions 910 and 920 in which the LINOX 940 has been annealed in accordance with one embodiment of the present invention. Annealing of the LINOX has increased the density of the LINOX, reduced the stresses between the LINOX and the semiconductor active area. The gouging and resultant dislocations that may occur at points 950 during poly/spacer etch have been eliminated. As a result, the problems caused by poly/spacer etch over active areas with sharp corners no longer exist. Thus, prior limitations placed on the topology of poly lines have been eliminated.

The preferred embodiment of the present invention, a process for reducing leakage in a SRAM cell with shallow trench isolated active areas, is thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.